International Journal of Electronics and
Communication Engineering (IJECE)
ISSN(P): 2278-9901; ISSN(E): 2278-991X
Vol. 3, Issue 3, May 2014, 31-38
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International Academy of Science,
Engineering and Technology
Connecting Researchers; Nurturing Innovations
IASET

IMPLEMENTATION OF FEED FORWARD NEURAL NETWORK MODULES USING CMOS DESIGN APPROACH

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ABSTRACT

This paper we design an analog circuit implementation, based on a CMOS technology, of the feed forward neural primitives of an on-chip learning architecture implementation approach. Basically our approach is based on current mode computation and is aimed at a low power / low voltage circuit implementation; moreover, it is easily scalable to implement network of any size. TANNER Tool efficient software for the VLSI design is utilized. Schematic of the circuit is designed on S-edit and then its respective output waveform viewed with W-edit. Utilizing Layer edit IC design is fabricated and simulation is successfully done with T-Spice**.**

KEYWORDS: VLSI, T Spice, CMOS, MLP, TANNER Tool

INTRODUCTION

The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI [1]. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. This trend is expected to continue, with very important implications on VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth. The other important characteristic is that the information services tend to become more and more personalized, which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility.

Neural networks [2], [3], [4], [5] are very important for the solution of problems characterized by uncertainly, imprecision and noise. Moreover, their processing parallelism can be exploited to obtain high speed hardware implementations. In this framework, our research goal is to VLSI implementation of very fast neural network. To improve the speed of the system, specific training method with chip-on-the-loop will be studied. To this purpose, some theoretical investigations were also done to understand the relation between the hardware parameters and the performance of the neural networks. CMOS is the most widely used microelectronic design process and it is found in almost every electronic product. CMOS is highly useful as it is faster, cheap, and reliable and has less power consumption. In this synopsis we are also using the current mode CMOS technology.

The CMOS circuit implementation of the feed forward neural primitives of a generic Multi-Layer Perceptron (MLP) network is presented. Basically our approach is based on current mode computation and is aimed at a low power / low voltage circuit implementation; moreover, it is easily scalable to implement network of any size.

The main requirement for any network to be fabricated on a CMOS VLSI chip is that its basic building block should be MOSFET's. TANNER Tool efficient software for the VLSI design is utilized.

METHODOLOGY

Two different levels can be considered in the design flow of Feed Forward Neural Network (FFNN). The input trans conductor, and the neuron circuit. The neural architecture we refer here is two-layer and Multi-Layer Perceptron (MLP). Basically all algorithmic variables (except for the input variables) are coded by differential electrical variables: the computation is performed as current mode. Concerning the physical realization, a particular gate level circuitry must be selected, and the required building blocks must be identified. Finally, these building blocks can be implemented as an integrated circuit according to the VLSI implementation technique. The design tasks at each level can be supported by TANNER tool.

- **CMOS Current Mode Primitives for Feed Forward Neural Networks**

Here the analog circuit implementation, based on a CMOS technology, of the feed forward neural primitives of an on-chip learning architecture implementation approach is presented. These primitives can be used to implement a generic Multi-Layer Perceptron (MLP) based feed-forward network. Moreover we designed and implemented a Weight Perturbation (WP) on-chip learning circuit architecture, presented in that makes use of the feed forward circuits which will be detailed in the following. From the architectural point of view, our approach focuses on the following issues and adopts the corresponding solutions:

Modularity and scalability i.e.

- Normalization of variables with respect to the number of inputs, hidden and output neurons, etc.
- Programmability of the neuron transfer function,
- Usage of current mode signals to make easier the sums;
- Complete on-chip learning implementation i.e.: the external supervisor only gives the start and target signals,
- Robustness with respect to noise and technological spread of parameters i.e.: differential coding of information, accurate matching of components, current mode computation,
- Wide signal dynamic range i.e.: current mode computation,
- Low power / low voltage i.e.: weak inversion region of operation of devices, supply voltage in the range (2.5-3)V or lower,
- Tran linear based circuits,
- Implementation of normalized sums of currents: both for the synaptic output currents and the output error (i.e. target - output neuron) currents,
- Programmable neuron circuit gain;
- Tradeoff between power and area i.e.: the maximum transistor bias current was set to 500 n A.

Analog VLSI on-chip learning Neural Networks represent a mature technology for a large number of applications involving industrial as well as consumer appliances. This is particularly the case when low power consumption, small size and/or very high speed are required. This approach exploits the computational features of Neural Networks, the implementation efficiency of analog VLSI circuits and the adaptation capabilities of the on-chip learning feedback schema.

Many experimental chips and microelectronic implementations have been reported in the literature based on the research carried out over the last few years by several research groups. The author presents and discusses the motivations, the system and circuit issues, the design methodology as well as the limitations of this kind of approach. Attention is focused on supervised learning algorithms because of their reliability and popularity within the neural network research community. In particular, the Back Propagation and Weight Perturbation learning algorithms are introduced and reviewed with respect to their analog VLSI implementation.

- **Circuit Architecture**

In figure 1, the circuit architecture of the feed forward network is illustrated: the neural architecture we refer to is the two-layer and Multi-Layer Perceptron (MLP). Basically all algorithmic variables (except for the input variables) are coded by differential electrical variables: the computation is performed as current mode. Let us analyze to a deeper detail each block. In the following we will report also the experimental measurements on the test chip; its voltage supply was set to 2.5V and the signal ground to 1.25V.

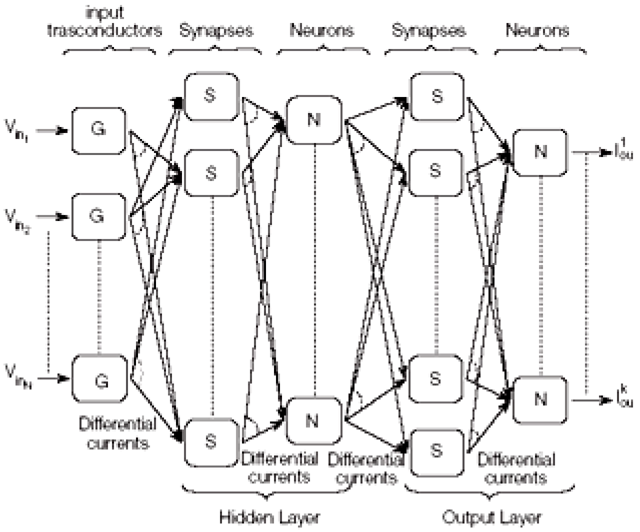

Figure 1: Circuit Architecture of the Feed Forward Network

- **The Input Trans Conductor**

The input blocks *G* in figure 1 are linearized trans conductors. They translate the single ended voltage mode inputs into differential balanced current mode signals varying in the range (-125 nA to + 125 n A)

The circuit implementation is detailed in figure 2. The transfer characteristic of the input differential pair is linearized by the voltage-controlled degenerating “resistors” (transistors *M*2 and *M*3 in figure 2)

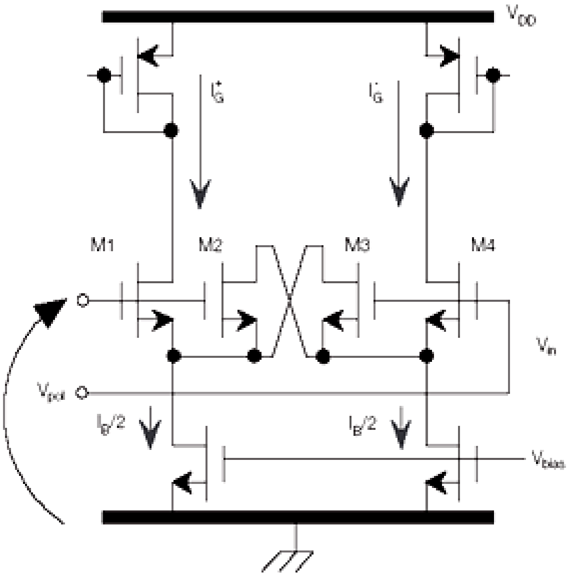

Figure 2: The Input Trans Conductor Circuit Schematic

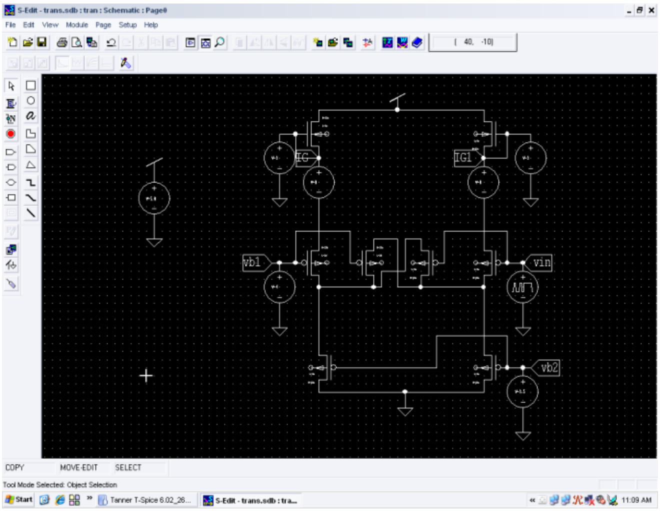
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Figure 2.1: Input Trans Conductor Design in S-Edit

- **The Neuron Circuit**

  The feed forward neuron circuit (blocks *N* in Figure 1) is composed of two blocks:

- The neuron transfer function slope control block (see the dashed box *A* in Figure 3);
- The neuron transfer function block (see the dashed box B in Figure 3). The circuit blocks are implemented as trans linear circuits.
- **The Neuron Transfer Function Slope Control Block:** To furtherly increase the modularity of the architecture, the slope of the neuron transfer function is programmable through a current mode control signal; the trans linear loop TL1 implements this functionality.
- **The Neuron Transfer Function Block:** The neuron transfer function block applies a sigmoidal shape transfer function to the current (*I*1 to*I*2). Each current component varies in the range [0 to 250 n A] and the differential neuron output current ($I_{Out}=I^{+}_{Out}-I^{-}_{Out}$) varies in the range [–250 nA to + 250 n A].

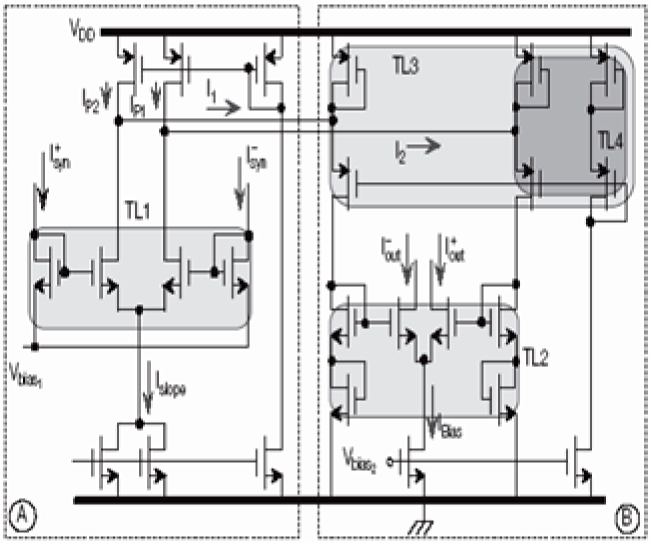

Figure 3: The Neuron Circuit Blocks Diagram

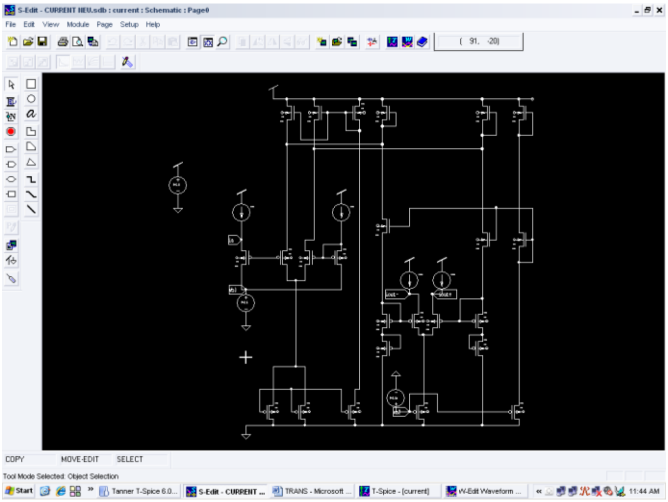
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Figure 3.1: The Neuron Circuit in S-Edit

RESULTS AND DISCUSSIONS

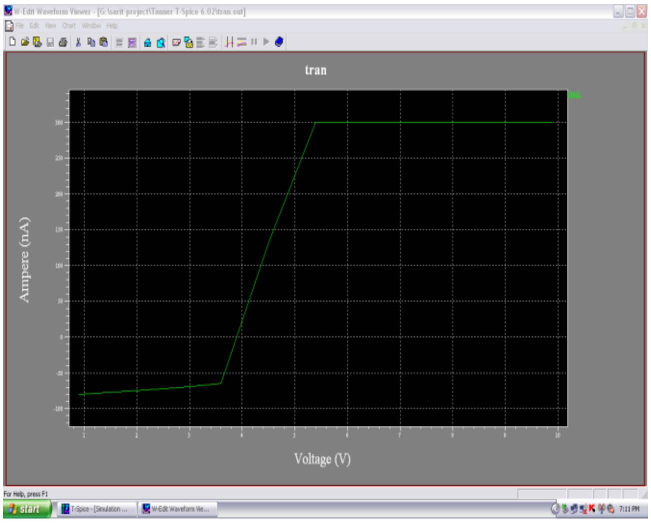
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Figure 4: Input Trans Conductor Output in W-Edit

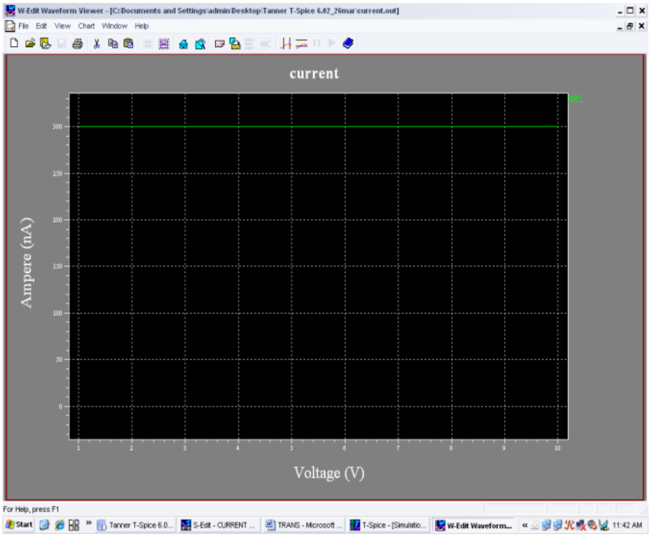

Figure 5: The Neuron Circuit Result in W-Edit

The input trans conductor circuit suitable for modeling neurons rather than neuron circuit in VLSI implementations of artificial neural networks (NN) is implemented using TANNER tool in S-Edit. The result of input trans conductor and neuron circuit are shown in the figure 4 and figure 5 respectively. From the output of the two methods we are ensure that the trans conductor output is more efficient than the neuron circuit. It generates an output voltage which is a sigmoidal-like function of the linear sum of a number of weighted inputs as shown in the figure 4. The weight of each input is individually controlled by a bias voltage which can be varied continuously and dynamically. Large numbers of these cells can be fashioned in regular arrays. It appears to be efficient because each weighted connection is implemented with only two MOSFET transistors. Butin case of neuron circuit instead of sigmoidal function it give an step function, which is not effective in the case of artificial neural network.

CONCLUSIONS

The feed forward neural networks are designed using CMOS VLSI technology. The tool selected for VLSI design of Fuzzy Logic Controller is the Tanner Tool. All the blocks of Fuzzy Logic Controller are designed in S-Edit & L-Edit and simulation is done in T-Spice. The output waveforms are viewed using W-Edit. The feed forward neural network is used for the design of character recognition circuit of I-POD. VLSI is faster, reliable and cheaper. So, the instantaneous reaction of system when the obstacle is sensed is obtained using VLSI. So, this system is highly useful in real time application. Due to less power dissipation in VLSI system has significant cost saving. So, in this way the feed forward type network is designed in VLSI using neural network. In the coming decades, feed forward neural networks will serve various useful purposes in field of character recognition, image compression, medicine, and electronic nose, security, and loan applications

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